

Performance of an ATM LAN Switch with Back-pressure Function

Hiroyuki Ohsaki, Naoki Wakamiya, Masayuki Murata and Hideo Miyahara

**Department of Information and Computer Sciences
Faculty of Engineering Science
Osaka University, Toyonaka 560, Japan**

**(Phone) +81-6-850-6588
(Fax) +81-6-850-6589
(E-mail) oosaki@ics.es.osaka-u.ac.jp**

Abstract

Traffic control schemes for ATM networks can be classified into two categories: reactive congestion control and preventive congestion control. Reactive congestion control can be effective in ATM local area networks as well as preventive congestion control. A possible scheme to realize efficient reactive congestion control is a switch architecture, which possesses buffers on both sides of input and output ports with a back-pressure function. Especially, when this switch is applied to ATM LANs for data transfer services, its performance should be evaluated by taking into account the bursty traffic, which is a main purpose of the current paper.

In this paper, we show the maximum throughput, the packet delay distribution, and the approximate packet loss probability of such an ATM switch with back-pressure function under bursty traffic through an analytic method. In addition to a balanced traffic condition, unbalanced traffic and a mixture of bursty and stream traffic are also considered. Through numerical examples, we show the effects of the average packet length and the output buffer size on the performance of the switch quantitatively.

Key words: ATM LAN, Input and Output Buffer switch, Back-pressure Function, Bursty Traffic

Contents

1	Introduction	3
2	Analytic Model	4
3	Derivation of Steady State Probability	6
4	Maximum Throughput Analysis	9
4.1	Case of Balanced Traffic condition	9
4.2	Case of Unbalanced Traffic at Output Ports	10
4.3	Case of Unbalanced Traffic at Input Ports	11
4.4	Case of Mixture with Stream Traffic	13
5	Derivation of Packet Delay Distribution	14
5.1	Switching Delay	15
5.2	Packet Waiting Time at Input Buffer	17
5.3	Packet Waiting Time at The Output Buffer	19
5.4	Numerical Examples	19
6	Approximate Analysis of Packet Loss Probability	20
6.1	Case of FIFO Switch	20
6.2	Case of RIRO Switch	21
6.3	Numerical Examples	22
7	Conclusion	23

1 Introduction

An ATM (Asynchronous Transfer Mode) technology realizes B-ISDN (Broadband Integrated Services Digital Network) by asynchronously treating various multimedia information such as data, voice and video. The benefit of the ATM technique is enjoyed by a statistical multiplexing of multimedia traffic by dividing it into fixed size packets (called cells). Much efforts of researches, developments and standardizations have been extensively devoted to public wide area ATM networks. In addition, the ATM technology also seems to be promising for realization of new high speed local area networks (LANs) to cope with a rapid advance of high-speed and multimedia-oriented computers.

Traffic control is an important issue for an efficient utilization of network resources in an ATM based network including wide and local area networks. Traffic control schemes can be classified into two categories; reactive congestion control and preventive congestion control. The reactive congestion control is the way to resolve network congestion after its occurrence. The preventive congestion control is, on the contrary, to prevent a network from its falling into congestion. The latter is now widely recognized as an effective way in wide area networks since the propagation delay is not negligible and QOS (Quality Of Service) requirements should be preserved in a strict manner. In ATM LANs, however, the propagation delay is small and is used in a private environment. Hence, preventive congestion control becomes meaningful because of its easier implementation.

To implement preventive congestion control in ATM LANs, Fan et al. recently proposes a switch architecture which possesses buffers on both sides of input and output ports with a back-pressure function [1]. The back-pressure function is provided to avoid a temporary congestion by prohibiting transmission of cells from input buffer to output buffer when the number of cells in output buffer exceeds a some threshold value. The performance of this kind of the switch has been analyzed by Iliadis in [1, 2, 3]. However, he assumed that interarrival times of cells at each input port follow a geometric distribution. Especially when the above switch is applied to ATM LANs for supporting data transfer service, its performance should be evaluated by taking into account the bursty nature of arriving traffic, i.e., packets coming from the upper protocol layers. In this paper, we show the performance of an ATM LAN switch with back-pressure function against bursty traffic, that is, the continuously arriving cells (forming a packet) which are destined for the same output port are treated for the analysis.

This paper is organized as follows. In section 2, an analytic model of the ATM switch we will evaluate is described. In section 3, the steady state probability of our model is derived. In section 4, the maximum throughput is derived based on the results of sections 3. Our subjects of investigation are extended to an imbalance traffic at input and output ports, and a mixture with stream traffic as well. In section 5, we derive the packet delay distribution. In section 6, the packet loss probability is derived by utilizing a Gaussian approximation. Finally, in section 7, we conclude our paper with some remarks.

2 Analytic Model

In this section, we describe an ATM LAN switch with back-pressure function followed by an introduction of our analytic model. The number of input ports (and output ports) is assumed to be N . Our ATM switch is equipped with buffers at both sides of input and output ports (see Fig. 1), and the buffer sizes are defined as N_I and N_O , respectively. The switching speed of cells from input buffer to output buffer is N times faster than the link speed, that is, at most N cells may be transferred from input buffer to output buffer

in a time slot. It is called the back-pressure function to prohibit transmission of cells from input buffer to output buffer by signaling back from output buffer to input buffer when the number of cells in output buffer exceeds a some predefined threshold value [4]. By this control, a cell overflow at output buffer can be avoided (see Fig. 2). However, it introduces HOL (Head Of Line) blocking of cells at input buffer, which results in the limitation of the switch performance.

We assume that a stream of successively arriving cells forms a packet, and the number of cells in the packet follows a geometric distribution with mean \overline{BL} . Let p denote the probability that a newly arriving cells belong to the same packet which is arriving at same input port. Thus, we have a relation;

$$\overline{BL} = \sum_{i=1}^{\infty} ip^{i-1} = \frac{1}{1-p} \quad (1)$$

We will assume that all cells are stored under first-in-and-first-out (FIFO) discipline at input buffer.

The practical threshold value at output buffer would be $N_O - N$ as proposed in [4]. However, as an ideal case, we assume that the HOL cells are transferred from input buffer to output buffer at random until the output buffer is filled up. In other words, when the output buffer is fully occupied with cells, input buffers which have HOL cells destined for that output buffer receives the back-pressure signal to stop cell transmission. Then, all HOL cells are awaited at the head of each input buffer. As soon as the cell in output buffer are transmitted onto the output link, one of HOL cells is selected at random and transmitted to the output buffer. Therefore, it is considered that HOL cells destined for the same output port form a virtual queue which we will call a HOL queue. While HOL cells are actually stored at the HOL queue, it can be regarded that HOL packets form the HOL queue in our modeling. Therefore, in what follows, we will use ‘‘HOL cell’’ and ‘‘HOL packet’’ without discrimination.

The switch size N will be assumed to be infinity in the following analysis. By introducing the assumption of the infinite switch size, we can focus on one single output port and its associated HOL queue. The infinite switch size gives the performance limitation as shown in [2, 5]. For example, when compared with the finite case, the maximum throughput with the infinite case gives an upper limit. Further, it is known that the close value are obtained when N reaches at 16 or 32 when the cell interarrivals follow a geometric distribution [2]. In this paper, we will examine this fact in the case of bursty traffic in section 4.

In this paper, we will first assume the capacity of the input buffer N_I to be infinity in obtaining the maximum throughput and the packet delay distribution. This assumption is realistic because the memory speed of the output buffer should be N times faster than the link speed. Thus, the capacity of the output buffer should be limited. On the other hand, the input buffer can be operated at the same speed as the link, which results in that the large capacity can be equipped. However, this assumption is relaxed for deriving the packet loss probability. As shown in section 6, the analysis will be appropriate however it can be expected accurately in the case of the large buffer size. In what follows, we consider a discrete time system in which its slot time equals to a cell transmission time on the input / output link.

Under assumptions described in the above, the system state is represented by two random variables Q_k and H_k , where Q_k is the number of cells at some output buffer and H_k is the number of HOL cells at input buffers associated with that output buffer, respectively. In the next section, the steady state probability of the doublet of two random variables (Q_k, H_k) is derived.

3 Derivation of Steady State Probability

In the following sections, we focus on a single output port and its associated HOL queue without loss of generality. Let H_k and Q_k denote the random variables for the number of HOL cells and the number of cells in the output buffer at k -th slot, respectively. We further introduce A_k for a random variable to represent the number of HOL packets newly arriving at the HOL queue at the beginning of k -th slot. By defining a symbol $(x)^+ = \max(0, x)$, we have the following equations.

1. $H_{k-1} + A_k \leq N_O - (Q_{k-1} - 1)^+$, that is, all HOL cells can be transferred to the output port:

At first, we have

$$Q_k = (Q_{k-1} - 1)^+ + H_{k-1} + A_k \quad (2)$$

Let B_k be the number of the HOL packets which further generate HOL cells at the current k -th slot. When there exist i HOL packets in HOL queue, the probability that B_k becomes j is:

$$b_{i,j} = \binom{i}{j} p^j (1-p)^{i-j}, \quad (3)$$

and we have

$$H_k = B_k. \quad (4)$$

2. $H_{k-1} + A_k > N_O - (Q_{k-1} - 1)^+$, that is, some HOL cells cannot be transferred to the output port at k -th slot:

$N_O - (Q_{k-1} - 1)^+$ HOL cells are transferred to the output buffer, and C_k cells out of them further generate HOL cells in the current k -th slot. Therefore, $H_{k-1} + A_k - (N_O - (Q_{k-1} - 1)^+)$ cells are kept waiting at the HOL queue. Hence,

$$Q_k = N_O \quad (5)$$

$$H_k = H_{k-1} + A_k - (N_O - (Q_{k-1} - 1)^+) + C_k \quad (6)$$

Since the switch size N is assumed to be infinity, arrivals of packets at input ports in time slot are assumed to follow a Poisson distribution [5]. Therefore,

$$a_j \equiv P[A = j] = P[A_k = j] = \frac{\lambda_p^j e^{-\lambda_p}}{j!} \quad (7)$$

In the above equation, λ_p is the mean arrival rate of packets at each input port. By defining λ_c as the mean arrival rate of cells at input ports, we have

$$\lambda_c = \lambda_p \overline{BL} \quad (8)$$

Now, we consider $s_{n,m,n',m'}$, the transition probability from state $[Q_{k-1} = n, H_{k-1} = m]$ to state $[Q_k = n', H_k = m']$. The transition probability $s_{n,m,n',m'}$ is obtained as follows.

1. When $n' < N_O$, that is, when the back-pressure function is not utilized:

From eq. (2), we have

$$A_k = Q_k - (Q_{k-1} - 1)^+ - H_{k-1} \quad (9)$$

When m' packets of $Q_k - (Q_{k-1} - 1)^+$ HOL packets further generate cells at the next slot, we have a relation

$$s_{n,m,n',m'} = a_{n'-(n-1)^+-m} b_{n'-(n-1)^+,m'} \quad (10)$$

2. When $n' = N_O$, that is, when the back-pressure function is used:

From eq. (6), we have

$$A_k = N_O - (Q_{k-1} - 1)^+ - H_{k-1} + (H_k - C_k) \quad (11)$$

Since C_k packets of $N_O - (Q_{k-1} - 1)^+$ HOL packets further generate cells at the next slot, we have a relation

$$s_{n,m,n',m'} = \sum_{i=0}^{m'} a_{n'-(n-1)^+-m+i} b_{n'-(n-1)^+,m'-i} \quad (12)$$

Once we have $s_{n,m,n',m'}$, the steady state probability $r_{n,m}$,

$$r_{n,m} = \lim_{k \rightarrow \infty} P[Q_k = n, H_k = m] = P[Q = n, H = m] \quad (13)$$

is obtained from eqs. (10) and (12).

1. When the state is $[Q = 0, H = 0]$, the output port becomes idle, i.e., we have

$$r_{0,0} = 1 - \rho \quad (14)$$

where ρ is defined as the maximum throughput normalized by the link capacity. By our assumption that the size of the input buffer is infinity, the maximum throughput ρ is equivalent to the cell arrival rate λ_c in steady state if it exists.

2. By considering all states that may be changed to state $[Q = n - 1, H = 0]$, we have (see Fig. 3)

$$r_{n,0} = \frac{1}{s_{n,0,n-1,0}} \left\{ r_{n-1,0} - \sum_{i=0}^{n-1} \sum_{j=0}^i s_{i,j,n-1,0} r_{i,j} \right\} \quad (0 < n \leq N_O) \quad (15)$$

3. By considering all states that may be changed to state $[Q = n, H = m]$, we have (see Fig. 4)

$$r_{n,m} = \frac{1}{1 - s_{n,m,n,m}} \left\{ \sum_{i=0}^{n-1} \sum_{j=0}^i s_{i,j,n,m} r_{i,j} + \sum_{k=0}^{m-1} s_{n,k,n,m} r_{n,k} \right\} \quad (0 < m, n < N_O) \quad (16)$$

4. By considering all states that may be changed to the state $[Q = N_O, H = m - 1]$, we have (see Fig. 5)

$$r_{N_O,m} = \frac{1}{s_{N_O,m,N_O,m-1}} \left\{ r_{N_O,m-1} - \sum_{i=0}^{N_O-1} \sum_{j=0}^i s_{i,j,N_O,m-1} r_{i,j} - \sum_{k=0}^{m-1} r_{N_O,k} \right\} \quad (0 < m) \quad (17)$$

4 Maximum Throughput Analysis

In this section, we obtain the maximum throughput using the steady state probability derived in section 3, under balanced traffic condition in subsection 4.1, under output unbalanced traffic condition in subsection 4.2, and under input unbalanced traffic condition in subsection 4.3. We will further consider the case of a mixture of bursty and stream traffic in section 4.4.

4.1 Case of Balanced Traffic condition

In this subsection, a balanced traffic condition is assumed, that is, a mean packet arrival rate at every input ports is identical and each packet determines its output port with an equal probability $1/N$.

In order to obtain the maximum throughput of our ATM switch, we consider the case where all input ports are saturated so that packets are always waiting in HOL queues. In this case, we have

$$\sum_{i=1}^N A^i = N - \sum_{i=1}^N H^i \quad (18)$$

where A^i is the random variable which represents the number of arriving packets destined for output port i in a slot and H^i is the random variable for the number of HOL cells destined for output port i . By dividing the above equation by N and letting N to be infinity, we have

$$\lambda_p = 1 - \overline{H} \quad (19)$$

where \overline{H} is the average number of HOL cells, and can be expressed with $r_{n,m}$ derived in section 3 as

$$\overline{H} = \sum_{n=0}^{N_O} \sum_{m=1}^{\infty} m r_{n,m} \quad (20)$$

From eqs. (8) and (19), we have

$$\lambda_c = (1 - \overline{H})\overline{BL} \quad (21)$$

The maximum throughput ρ can be obtained by substituting λ_c in the above equation with ρ and solving it for ρ . Since \overline{H} depends on ρ , ρ is solved iteratively by virtue of a standard iteration technique such as a bisection method [6].

In Figs. 6 and 7, the maximum throughput ρ is plotted against the average packet length \overline{BL} and the output buffer size N_O , respectively. These figures show that the packet length drastically degrades the maximum throughput. Further, we may observe that the size of output buffers must be larger than the average packet length to gain a sufficient throughput. Fig. 8 shows the simulation results in the case where the switch size is finite for $N_O = 1$ and $N_O = 50$. The results of the analysis become slightly smaller than those of the simulation. Here, we note that the maximum throughput for $N_O = 1$ is exactly same as a well known value of input queueing, 0.585 [5].

4.2 Case of Unbalanced Traffic at Output Ports

In this section, output unbalanced traffic is treated following the approach presented in [1]. Output buffers are divided into two groups called O_1 and O_2 . Let q_O be a ratio of the number of output ports belonging to the group O_1 as:

$$q_O \equiv \frac{|O_1|}{N} \quad (22)$$

The packet arrival rate at each input port is identical. However, each packet arriving at the input port selects one of output ports in group O_1 with probability P_{G1} or one of output ports in group O_2 with probability P_{G2} . By assuming $P_{G1} \geq P_{G2}$ without loss of generality, the relative probability r_O is denoted as

$$r_O \equiv \frac{P_{G1}}{P_{G1} + P_{G2}} \geq 0.5 \quad (23)$$

It is noted that the balanced traffic case is a special case by setting $q_O = 0$, $q_O = 1$ or $r_O = 0.5$. Let P_1 and P_2 be the probabilities that an arriving packet is destined to an output port belonging to the O_1 and O_2 , respectively, we have from eqs. (22) and (23),

$$P_1 = \frac{q_O r_O}{1 - q_O - r_O + 2q_O r_O} \quad (24)$$

$$P_2 = \frac{1 - q_O - r_O + q_O r_O}{1 - q_O - r_O + 2q_O r_O} \quad (25)$$

where λ_p is defined as the packet arrival rate at input ports, and λ_{p1} and λ_{p2} are the packet arrival rates at output ports belonging to the group O_1 and O_2 , respectively. We then obtain

$$\lambda_{p1} = \frac{r_O \lambda_p}{1 - q_O - r_O + 2q_O r_O} \quad (26)$$

$$\lambda_{p2} = \frac{(1 - r_O) \lambda_p}{1 - q_O - r_O + 2q_O r_O} \quad (27)$$

For deriving the maximum throughput, we consider a relation:

$$\sum_{i=1}^N A^i = N - \left(\sum_{i=1}^{|O_1|} H_1^i + \sum_{i=1}^{|O_2|} H_2^i \right) \quad (28)$$

where random variables H_1^i (H_2^i) is the number of HOL cells destined for the output port belonging to the group O_1 (O_2). By dividing the above equation by N and letting N to be infinity, we have

$$\lambda_p = 1 - \{q_O \bar{H}_1 + (1 - q_O) \bar{H}_2\} \quad (29)$$

where \bar{H}_1 and \bar{H}_2 are the average number of HOL cells destined for the group O_1 and O_2 , respectively. From eq. (8), we have

$$\lambda_c = \left[1 - \{q_O \bar{H}_1 + (1 - q_O) \bar{H}_2\} \right] \bar{BL} \quad (30)$$

The maximum throughput ρ can be obtained by substituting λ_c in the above equation with ρ and solving for ρ in the same manner presented in section 4.1.

In Figs. 9 and 10, the relations between q_O and the maximum throughput are plotted for $\bar{BL} = 1$ and $\bar{BL} = 10$, respectively. These figures show that an unbalanced traffic and a larger packet size cause degradation of the maximum throughput.

4.3 Case of Unbalanced Traffic at Input Ports

In this subsection, we evaluate the performance of the switch under the unbalanced traffic condition at the input ports. Similarly to the previous subsection, input ports are divided into two groups I_1 and I_2 . Let q_I be a ratio of the number of input ports belonging to the group I_1 defined as:

$$q_I \equiv \frac{|I_1|}{N} \quad (31)$$

λ_{p1} and λ_{p2} are mean packet arrival rates at the groups I_1 and I_2 , respectively. Assuming that $\lambda_{p1} \geq \lambda_{p2}$ is assumed without loss of generality, we introduce r_I as;

$$r_I \equiv \frac{\lambda_{p1}}{\lambda_{p1} + \lambda_{p2}} \geq 0.5 \quad (32)$$

It is noted that the balanced traffic case is the special case by setting $q_I = 0$, $q_I = 1$ or $r_I = 0.5$. We assume that each packet arriving at the input port chooses the output port with a same probability $1/N$. By letting λ_p denote the packet arrival rate at each output port, λ_{p1} and λ_{p2} are given as:

$$\lambda_{p1} = \frac{\lambda_p r_I}{1 - q_I - r_I + 2q_I r_I} \quad (33)$$

$$\lambda_{p2} = \frac{\lambda_p (1 - r_I)}{1 - q_I - r_I + 2q_I r_I} \quad (34)$$

To obtain the maximum throughput, we consider the case where input ports are saturated. Recalling that we assume $\lambda_{p1} \geq \lambda_{p2}$, the input buffers belonging to the group I_1 is saturated first. Thus, we have a relation:

$$\sum_{i=1}^{|O_1|} A_1^i = |O_1| - \sum_{i=1}^{|O_1|} H^i \quad (35)$$

where the random variable A_1^i is the number of packets arriving at input port i belonging to the group I_1 . By dividing the above equation by N and letting N to be infinity, we have

$$\lambda_{p1} = 1 - \overline{H} \quad (36)$$

From eq. (8), the following relation holds.

$$\lambda_{c1} = (1 - \overline{H}) \overline{BL} \quad (37)$$

where λ_{c1} is the mean packet arrival rate at each input port belonging to the group I_1 . The maximum throughput ρ can be obtained by substituting λ_{c1} in the above equation with ρ and solving for ρ as in the same manner presented in subsection 4.1.

Figs. 11 and 12 show the maximum throughput dependent on q_I for $\overline{BL} = 1$ and $\overline{BL} = 10$, respectively. These figures show that an unbalanced traffic condition and a larger packet size degrade the maximum throughput. The result for $\overline{BL} = 1$ is almost same as that for output unbalanced traffic (see Fig. 9). On the other hand, the result for $\overline{BL} = 10$ show higher performance than that of output unbalanced traffic (see Fig. 10). This is because unbalanced traffic at input ports causes less HOL blocking than at output ports.

4.4 Case of Mixture with Stream Traffic

Finally, we derive the maximum throughput in the case where the bursty traffic and the stream traffic coexist. Here, we assume that the stream traffic occupies some portion of the link with constant peak rate. For example, this class of traffic can support an uncompressed video transfer service.

Let R denote the peak rate of stream traffic normalized by the link capacity. The switch can simultaneously accept m ($\leq \lfloor 1/R \rfloor$) calls of stream traffic. We assume that call arrivals of the stream traffic follow a Poisson distribution with mean λ_{CBR} , and its service time (or call holding time) does an exponential distribution with mean $1/\mu_{CBR}$. While both bursty and stream traffic share a link, cells from the stream traffic are given a higher priority. Namely, cells from stream traffic arriving at the input port are transferred to its destined output port prior to cells from bursty traffic [4]. By this control mechanism, it can be considered that bursty traffic can utilize $1 - nR$ of the link capacity when n calls of stream traffic are accepted. We note here that if compressed video transfer service is accommodated as stream traffic, a more capacity can be utilized by the bursty traffic. Thus, the maximum throughput derived in the below should be regarded as the “minimum” guaranteed throughput for the bursty traffic.

Since the stream traffic is given a high priority, it can be modeled by a M/M/m/m queueing system. By letting π_n be the probability that n calls of stream traffic are accepted in steady state, we have (e.g., [7])

$$\pi_n = \left[\sum_{n=0}^m \left(\frac{\lambda_{CBR}}{\mu_{CBR}} \right)^n \frac{1}{n!} \right]^{-1} \left(\frac{\lambda_{CBR}}{\mu_{CBR}} \right)^n \frac{1}{n!} \quad (38)$$

Since the service time of steam traffic can be assumed to be much longer than cell or the packet transmission time of bursty traffic, an available link capacity to bursty traffic is regarded to be constant when the number of accepted calls of stream traffic is fixed. By letting ρ_n be the maximum throughput for bursty traffic when n calls of the stream traffic are accepted, we have [4]

$$\rho_n = (1 - nR)\rho \quad (39)$$

where ρ is defined as the maximum throughput of bursty traffic when all link capacity is allocated to bursty traffic, and has been already derived in subsection 4.1. Consequently, the “averaged” maximum throughput ρ' is:

$$\rho' = \sum_{n=0}^m \pi_n \rho_n \quad (40)$$

Fig. 13 shows the maximum throughput of bursty traffic and stream dependent on an offered traffic load for stream traffic for $N_O = 50$, $\mu_{CBR} = 0.1$, $R = 0.2$ and $m = 5$. From this figure, we can observe the natural idea that the larger the average packet length is, the smaller the maximum allowable throughput of bursty traffic is. Therefore, the available bandwidth allocated to the stream traffic should be limited in some way to avoid a degradation of bursty traffic efficiency to some degree. One possible approach is to decrease m , the maximum number of calls of stream traffic that the switch can accept. In Fig. 14, the maximum throughput of both bursty traffic and stream traffic dependent on the offered traffic load for stream traffic for $\overline{BL} = 1$ and several values of m . It shows that the performance degradation of bursty traffic can be avoided to some extent by limiting m .

5 Derivation of Packet Delay Distribution

In this section, we derive the derivation of the packet delay experienced at input buffer and at output buffer. The packet delay is defined as the time duration from when its first cell of the packet arrival at the input port of the switch to when the last cell is transmitted onto the output link. We divide the packet delay into the following three elements.

1. W_I : The packet waiting time at the input buffer from the arrival time of the first cell of the packet at the input buffer to its arrival time at the HOL queue.
2. W_S : The switching delay from the HOL queue to its destination output port; i.e., the time duration from the arrival time of the first cell at the HOL queue to the departure time of the last cell from the HOL queue.
3. W_O : The packet waiting time at the output buffer from the arrival time of the first cell at the output buffer to the departure time of the last cell from the output buffer.

It was assumed that the cell transmission from the HOL queue is performed by a random discipline for cells arriving in the same slot, and by a FIFO discipline for cells arriving in different slots. In the following subsections, we will derive the above three elements.

5.1 Switching Delay

For obtaining the switching delay W_S , we examine the cell transmission behavior of the tagged packet arriving at the HOL queue. Let u_m be the probability that the number of packets waiting in the HOL queue including the just arriving tagged packet equals to m , which is obtained as

$$u_m = \sum_{n=0}^{N_O} \sum_{j=1}^m r_{n,m-j} a'_j \quad (41)$$

where a'_j is the probability that the tagged packet arrives with j packets in the same slot, i.e.,

$$a'_j = \frac{j a_j}{\sum_{k=1}^{\infty} k a_k} = \frac{j a_j}{\lambda_p} \quad (42)$$

In what follows, we will refer a cycle to the time to transfer all cells of the tagged packet from the HOL queue to the output buffer.

Suppose now that there are m packets including the tagged one in the HOL queue at the beginning of the cycle, that j packets of them have more cells to transfer, and that $m' - 1 - j$ packets newly arrive at the HOL queue during the cycle. In this case, the transition probability $t_{m,m'}$ is given as:

$$t_{m,m'} = \sum_{j=0}^{m'-1} b_{m-1,j} a_{m'-1-j}^m \quad (43)$$

where a_k^m is defined as the probability that k packets arrives at the HOL queue during m slots, i.e.,

$$a_k^m = \frac{(\lambda_p m)^k e^{-\lambda_p m}}{k!} \quad (44)$$

Let $T_{m,m'}(k)$ be the cycle time distribution when m HOL cells exist at the beginning of the cycle, and when m' HOL cells does at the beginning of the next cycle. Using the above probability $t_{m,m'}$, $T_{m,m'}(k)$ is expressed as follows.

$$T_{m,m'}(k) = \begin{cases} t_{m,m'}, & \text{if } k = m \\ 0, & \text{otherwise} \end{cases} \quad (45)$$

By letting $T_{m,m'}^l(k)$ be the distribution over l cycles, we have:

$$T_{m,m'}^l(k) = \sum_{j=1}^{\infty} [T_{m,j}^{l-1} \otimes T_{j,m'}](k) \quad (46)$$

where a symbol \otimes is the convolution operator of two probability distributions. That is, for two probability distributions $y_1(k)$ and $y_2(k)$, it is defined as

$$[y_1 \otimes y_2](k) \equiv \sum_{j=0}^k y_1(j)y_2(k-j). \quad (47)$$

Next, let $U_m(k)$ represent the delay distribution of the last cell of the tagged packet. Because of our assumption that the cell transmission are done by a random discipline among cells arriving at the HOL queue in the same slot, we have

$$U_m(k) = \begin{cases} 1/m, & \text{if } 0 \leq k \leq m-1 \\ 0, & \text{otherwise} \end{cases} \quad (48)$$

We further introduce $W_m(k)$ which is denoted as the transmission time distribution of the tagged packet conditioned on m , which is the number of HOL packets when the tagged packet arrives at the HOL queue. Recalling that the packet length (the number of cells in the packet) follows a geometric distribution with parameter p , $W_m(k)$ is given by:

$$W_m(k) = (1-p)U_m(k) + \sum_{l=1}^{\infty} p^l(1-p) \sum_{j=1}^{\infty} [T_{m,j}^l \otimes U_j](k) \quad (49)$$

Hence, the mean switching delay W_S is obtained as

$$W_S = \sum_{m=1}^{\infty} \sum_{k=1}^{\infty} kW_m(k)u_m \quad (50)$$

5.2 Packet Waiting Time at Input Buffer

In order to obtain W_I , we first consider the random variable W_H , the time from when the first cell of the packet arrives at the HOL queue to when all cells belonging to the same packet are transferred to the output buffer. The derivation of distribution for W_H is similar to that of W_S , but in addition to the state of the HOL queue, the state of the output buffer should be taken into account. Let $u_{n,m}$ be the probability that there are

m packets in the HOL queue and n cells in the output buffer at the arriving instant of the tagged packet. It is determined as;

$$u_{n,m} = \begin{cases} \sum_{j=1}^m (r_{0,m-j} + r_{1,m-j}) a'_j, & \text{if } n = 0 \\ \sum_{j=1}^m r_{n+1,m-j} a'_j, & \text{otherwise} \end{cases} \quad (51)$$

We define $C_{n,m,n',m'}(k)$ as the probability distribution of a cycle time that the state was (n, m) at the beginning of a cycle, and that the state becomes (n', m') at the beginning of the next cycle. It is noted that the current definition of the cycle is different from that in the previous subsection in the sense that it is observed at the HOL queue. More precisely, when the output buffer has space to accept, say these cells, three cells can be transmitted simultaneously in one slot from the HOL queue if those exist, and in the current definition of the cycle, it is counted as one slot. On the other hand, in the previous subsection, it is counted as three slots to derive the switching delay. $C_{n,m,n',m'}(k)$ is obtained dependent on m and n as follows.

- $m \leq N_O - n$;

Since all HOL cells can be transferred to the output buffer, the cycle time is just one slot. The state of the output buffer then becomes $n' = n + m$. On the other hand, the number of HOL packets becomes $m' = j + k + 1$ when j of HOL packets (except the tagged one) have more cells to transfer and when k packets newly arrives in the current cycle. Consequently, we have

$$C_{n,m,n',m'}(k) = \begin{cases} \sum_{j=0}^{m'} b_{m-1,j} a_{m'-1-j}, & \text{if } k = 1 \text{ and } n' = n + m \\ 0, & \text{otherwise} \end{cases} \quad (52)$$

- $m > N_O - n$;

$N_O - n$ cells are transferred to the output buffer in one slot, and other $m - (N_O - n)$ cells are transferred continuously in the following slots. Therefore, the cycle time is $1 + m - (N_O - n)$, and the state of the output buffer becomes $n' = N_O$. When j packets of $m - 1$ HOL packets have more cells to transfer and when k packets arrive at the current cycle, the number of HOL packets becomes $m' = k + 1$. Therefore, we have

$$C_{n,m,n',m'}(k) = \begin{cases} \sum_{j=0}^{m'} b_{m-1,j} a_{m'-1-j}^{m-(N_O-n)+1}, & \text{if } k = m - (N_O - n) \text{ and } n' = N_O \\ 0, & \text{otherwise} \end{cases} \quad (53)$$

The cycle time distribution over l cycles is then obtained;

$$C_{n,m,n',m'}^l(k) = \sum_{n''=0}^{N_O} \sum_{m''=1}^{\infty} [C_{n,m,n'',m''}^{l-1} \otimes C_{n'',m'',n',m'}](k) \quad (54)$$

Let $U_{n,m}(k)$ be the delay distribution of the last cell of the packet in the cycle. Because of our assumption that the cell transmission are done by a FIFO discipline among cells arriving in distinct slots, we have $U_{n,m}(k)$ as follows;

- $m \leq N_O - n$

$$U_{n,m}(k) = \begin{cases} 1, & \text{if } k = 0 \\ 0, & \text{otherwise} \end{cases} \quad (55)$$

- $m > N_O - n$

$$U_{n,m}(k) = \begin{cases} (N_O - n)/m, & \text{if } k = 0 \\ 1/m, & \text{if } k \leq m - (N_O - n) \\ 0, & \text{otherwise} \end{cases} \quad (56)$$

Probability distribution of W_H is finally obtained as:

$$W_H(k) = \sum_{n=0}^{N_O} \sum_{m=1}^{\infty} u_{n,m} \left[(1-p)U_{n,m}(k) + \sum_{l=1}^{\infty} p^l (1-p) \sum_{n'=0}^{N_O} \sum_{m'=1}^{\infty} [C_{n,m,n',m'}^l \otimes U_{n',m'}](k) \right] \quad (57)$$

The corresponding n -th moment $W_H^{(n)}$ is then given by

$$W_H^{(n)} = \sum_{k=1}^{\infty} k^n W_H(k) \quad (58)$$

By considering a Geom/G/1 queueing system where the first and second moments of the service time is given by $W_H^{(1)}$ and $W_H^{(2)}$, respectively, we have (see, e.g., [8])

$$W_I = \frac{\lambda_p W_H^{(2)}}{2(1 - \lambda_p W_H^{(1)})} \quad (59)$$

5.3 Packet Waiting Time at The Output Buffer

Since W_O means the delay of the first cell of the packet in the output buffer, we simply have

$$W_O = 1 + \sum_{n=1}^{N_O} \sum_{m=0}^{\infty} nr_{n,m} \quad (60)$$

including the transmission time of the last cell.

5.4 Numerical Examples

Figs. 15 and 16 show the relations between the offered load and the average packet delay for $\overline{BL} = 1$ and $\overline{BL} = 3$, respectively. These figures show that the large offered load suddenly increase the average packet delay, and at the point where the offered load reaches at the maximum throughput, the average packet delay becomes saturated. Thus, an appropriate size of the output buffer makes it possible to sustain the increase of the average packet delay.

6 Approximate Analysis of Packet Loss Probability

In this section, the packet loss probability is derived utilizing a Gaussian approximation. In addition to the FIFO switch considered above, the RIRO (Random-In-Random-Out) switch [4] is also considered. In the RIRO switch, all cells at each input buffer are stored in logically separated buffers, each of which is associated with the destination output port, in order to avoid the HOL blocking. The packet loss probabilities for these two switches are approximately derived in the followings.

6.1 Case of FIFO Switch

At first, we consider a discrete time Geom/G/1 queueing system where the packet interarrival times follow a geometric distribution with parameter λ_p . We define $\Lambda(z)$ as the probability generation function (PGF) for the distribution of the number of packets arriving in a slot, which is given by

$$\Lambda(z) = 1 - \lambda_p + \lambda_p z \quad (61)$$

Further, we let $B(z)$ be the PGF of probability distribution of the service time of the customers. Its i -th derivative is defined by $b^{(i)}$, i.e.,

$$b^{(i)} \equiv \left. \frac{d^i B(z)}{dz^i} \right|_{z=1} \quad (62)$$

The PGF of the unfinished work for this system is given as (see, e.g., [8]):

$$U(z) = \frac{(1 - \rho)(1 - z)\Lambda[B(z)]}{\Lambda[B(z)] - z} \quad (63)$$

where ρ is the utilization obtained as:

$$\rho = \lambda_p b^{(1)} \quad (64)$$

The average and the variance of $U(z)$ is derived as:

$$E[U] = \left. \frac{dU(z)}{dz} \right|_{z=1} = \frac{\lambda_p [2b^{(1)} - 2\lambda_p (b^{(1)})^2 + b^{(2)}]}{2(1 - \lambda_p b^{(1)})} \quad (65)$$

$$V[U] = u^{(2)} + E[U] - E[U]^2 \quad (66)$$

where $u^{(2)}$ is given by

$$u^{(2)} = \left. \frac{d^2 U(z)}{dz^2} \right|_{z=1} \quad (67)$$

$$= \frac{\lambda_p [6b^{(2)} - 6\lambda_p b^{(1)}b^{(2)} + 3\lambda_p (b^{(2)})^2 + 2b^{(3)} - 2\lambda_p b^{(1)}b^{(3)}]}{6(1 - \lambda_p b^{(1)})^2} \quad (68)$$

In the current system of the FIFO switch, we can view the number of cells in the input buffer as the unfinished work. Therefore, the packet loss probability P_L is approximately given as:

$$P_L(FIFO) \cong Pr[U > N_I] = \int_{N_I}^{\infty} \frac{1}{\sqrt{2\pi V[U]}} e^{-\frac{(y-E[U])^2}{2V[U]}} dy \quad (69)$$

where N_I represents the buffer size. The probability distribution of W_H obtained in section 5 can be applied to eq. (69) for the moments of the service time distribution. Namely, $b^{(i)}$'s ($1 \leq i \leq 3$) are given by

$$b^{(1)} = W_H^{(1)} \quad (70)$$

$$b^{(2)} = W_H^{(2)} - W_H^{(1)} \quad (71)$$

$$b^{(3)} = W_H^{(3)} - 3W_H^{(2)} + 2W_H^{(1)} \quad (72)$$

6.2 Case of RIRO Switch

We assume that each input buffer is composed of N Geom/G/1 queues, each of which is associated with the output port. We further assume that each queue is served independently. This assumption is realistic if the switch performs an appropriate cell transmission scheduling [4]. Furthermore, by assuming a balanced traffic load condition, the mean packet arrival rate at j -th queue at the input buffer (dedicated to the output port j) is given as

$$\lambda_j = \frac{\lambda_p}{N} \quad (73)$$

By letting $\Lambda_j(z)$ be the z -transform for the number of packets arriving in a slot, we have

$$\Lambda_j(z) = 1 - \lambda_j + \lambda_j z \quad (74)$$

We define V_j as a random variable for the number of cells waiting at j -th queue in the input buffer. To prevent a single queue from occupying the whole input buffer, the threshold value T_h is introduced for all queues, and the packet loss probability due to this threshold value T_h is given by

$$P(T_h) \cong Pr[V_j > T_h] \quad (75)$$

The packet service time distributions for each queue are obtained from eq. (72) by letting λ be λ_j , respectively.

Next, let U_N be the random variable to represent the unfinished work defined as

$$U_N = \sum_{j=1}^N V_j \quad (76)$$

By introducing $U_N(z) = V_j(z)^N$ for the PGF of U_N , the average and the variance of U_N are obtained as follows.

$$E[U_N] = \left. \frac{dV_j(z)}{dz} \right|_{z=1} \quad (77)$$

$$V[U_N] = E[U_N^2] + E[U_N] - E[U_N]^2 \quad (78)$$

Let P_L denote the probability that the number of cells at input buffer exceeds the physical buffer size N_j , we have

$$P_L(RIRO) \cong Pr\left[\lim_{N \rightarrow \infty} \sum_{j=1}^N V_j > N_{in}\right] = Pr\left[\lim_{N \rightarrow \infty} U_N > N_{in}\right] \quad (79)$$

Consequently, the packet loss probability for the RIRO switch, $P(RIRO)$, is obtained as follows.

$$P(RIRO) \cong \max(P(T_h), P_L(RIRO)) \quad (80)$$

6.3 Numerical Examples

In Figs. 17 and 18, the packet loss probabilities dependent on the offered load are plotted for $\overline{BL} = 1$ and $\overline{BL} = 3$, respectively. For comparison purposes, we also provide the result of the output buffer switch [5]. Here, we set $N_I + N_O = 30$ in the cases of FIFO and RIRO switches and $N_O = 30$ in the case of the output buffer switch. In both cases of FIFO and RIRO switches, the larger offered load results in sudden degradation of the packet loss probability. The FIFO switch shows the higher packet loss probability than the RIRO switch for the same buffer size due to HOL blocking. However, the FIFO switch can be implemented more easily, and its performance may be improved by large capacity of the input buffer, and it is superior to the output buffer switch when the offered load is limited to its maximum throughput. On the other hand, although the implementation of the RIRO switch would be more complicated, its performance is even higher than the output buffer switch.

7 Conclusion

In this paper, an ATM switch with input and output buffer equipped with back-pressure function was treated. We have analyzed its performance under bursty traffic condition for applying it to ATM LANs. We have derived the maximum throughput and the packet delay distribution as well as the approximate packet loss probability under the assumption that the switch size is infinite. Consequently, we have shown that larger packet lengths drastically degrade the performance of the switch. However, it is possible to sustain such a degradation to some extent by larger output buffers. At least, the output buffer size comparable to the average packet length is necessary to gain a sufficient performance.

Last, we note that our analytic approach described in the current paper can be applied to the other cases, e.g., the case where the switching speed is L ($1 \leq L \leq N$) times faster than the link speed (see, e.g., [9]), or the case where, when $L'(> L)$ cells are simultaneously destined for the same output buffer, $(L' - L)$ cells are lost or kept awaiting at the input buffer.

For further works, we should evaluate the performance of the network in which two or more ATM switches are interconnected. In such a network, even when a long term congestion introduces large queue length at the input buffer, cell losses may be avoided to send a back-pressure signal to the upper adjacent switches.

Acknowledgment

We would like to thank Dr. Hiroshi Suzuki and Dr. Ruixue Fan with NEC Corporation, C&C System Laboratories, for their invaluable suggestions.

References

- [1] I. Iliadis, "Performance of a packet switch with input and output queueing under unbalanced traffic," in *Proceedings of IEEE INFOCOM '92*, vol. 2, (Florence, Italy), pp. 743–752 (5D.4), May 1992.

- [2] I. Iliadis, "Head of the line arbitration of packet switches with input and output queueing," in *Fourth International Conference on Data Communication Systems and their Performance*, (Barcelona, Spain), pp. 85–98, June 1990.
- [3] I. Iliadis, "Synchronous versus asynchronous operation of a packet switch with combined input and output queueing," *Performance Evaluation*, no. 16, pp. 241–250, 1992.
- [4] K. Y. Ruixue Fan, Hiroshi Suzuki and N. Matsuura, "Expandable ATOM switch architecture (XATOM) for ATM lans," *ICC '94*, 5 1994.
- [5] M. J. Karol, M. G. Hluchyj, and S. P. Morgan, "Input vs. output queueing on a space-division packet switch," in *Proceedings of IEEE GLOBECOM '86*, (Houston, Texas), pp. 659–665, Dec. 1986.
- [6] S. A. T. William H. Press, Brian P. Flannery and W. T. Vetterling, *Numerical Recipes in C*. Cambridge University Press, 1988.
- [7] D. Bertsekas and R. Gallager, *Data Networks*. Englewood Cliffs, New Jersey: Prentice-Hall, 1987.
- [8] H. Takagi, *Queueing Analysis Volume 3: Discrete-Time Systems*. North-Holland, 1993.
- [9] Yuji Oie, Masayuki Murata, Koji Kubota, and Hideo Miyahara, "Performance analysis of nonblocking packet switches with input / output buffers," *IEEE Transactions on Communications*, vol. 40, pp. 1294–1297, August 1992.

List of Figures

1	The ATM switch with back-pressure function.	27
2	The analytic model.	27
3	State transition diagram in the case of $m = 0$ and $0 < n \leq N_O$	28
4	State transition diagram in the case of $0 < m$ and $n < N_O$	28
5	State transition diagram in the case of $0 < m$ and $n = N_O$	29
6	Maximum throughput vs. the average packet length.	29
7	Maximum throughput vs. the output buffer size.	30
8	Comparison with simulation results.	30
9	Unbalanced traffic at output ports ($N_O = 10, \overline{BL} = 1$).	31
10	Unbalanced traffic at output ports ($N_O = 10, \overline{BL} = 10$).	31
11	Unbalanced traffic at input ports ($N_O = 10, \overline{BL} = 1$).	32
12	Unbalanced traffic at input ports ($N_O = 10, \overline{BL} = 10$).	32
13	Throughput vs. the offered load of stream traffic.	33
14	Effect of an available link capacity limitation on stream traffic.	33
15	The average packet delay vs. the offered load for $\overline{BL} = 1$	34
16	The average packet delay vs. the offered load for $\overline{BL} = 3$	34
17	The packet loss probability vs. the offered load for $\overline{BL} = 1$	35
18	The packet loss probability vs. the offered load for $\overline{BL} = 3$	35

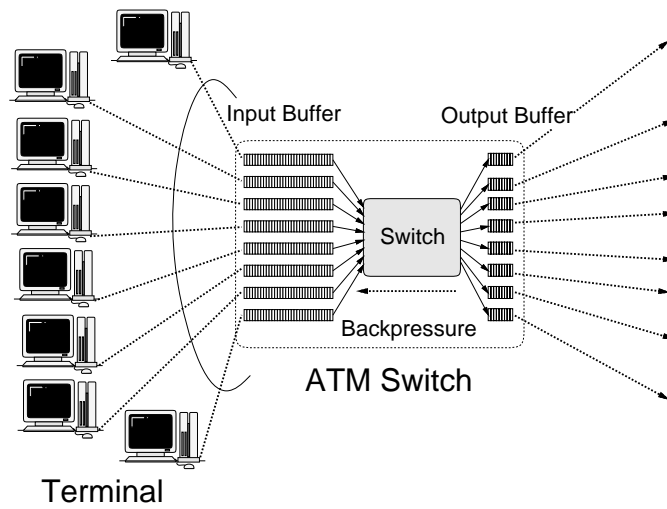


Figure 1: The ATM switch with back-pressure function.

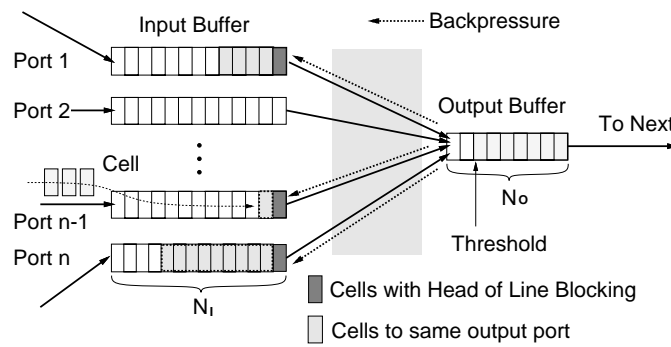


Figure 2: The analytic model.

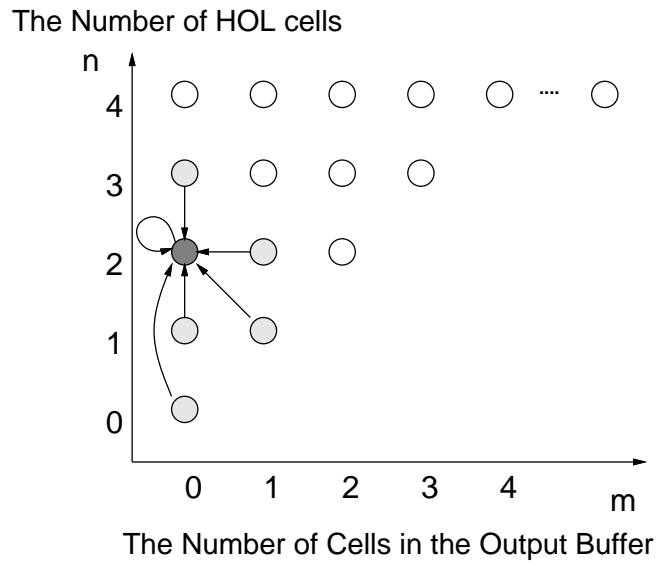


Figure 3: State transition diagram in the case of $m = 0$ and $0 < n \leq N_0$.

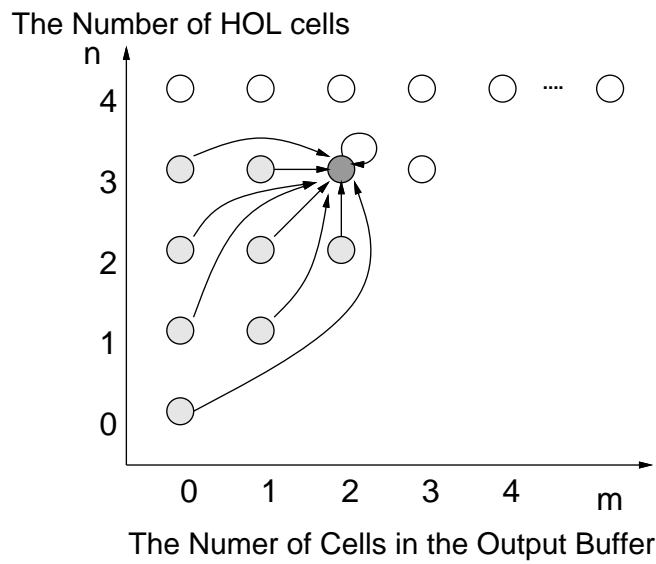


Figure 4: State transition diagram in the case of $0 < m$ and $n < N_0$.

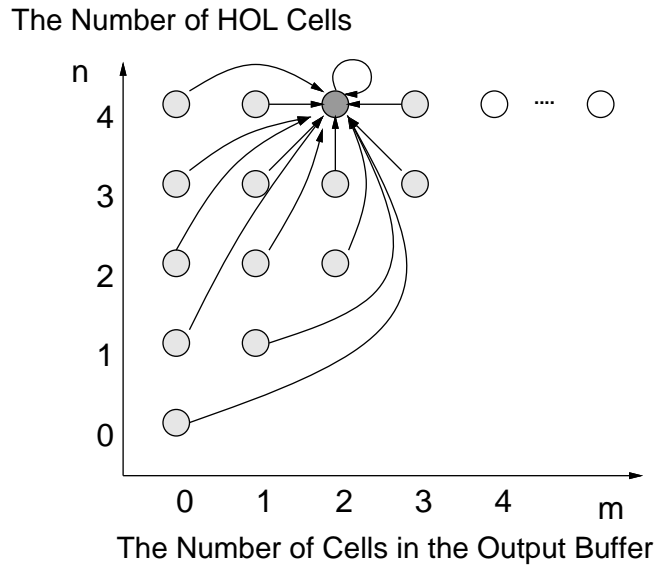


Figure 5: State transition diagram in the case of $0 < m$ and $n = N_O$.

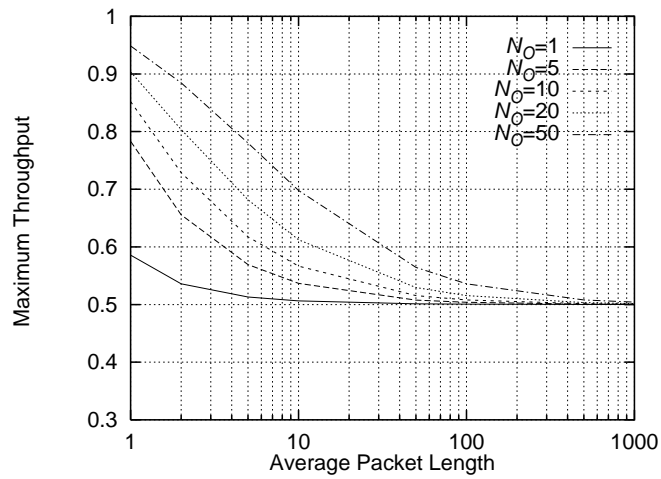


Figure 6: Maximum throughput vs. the average packet length.

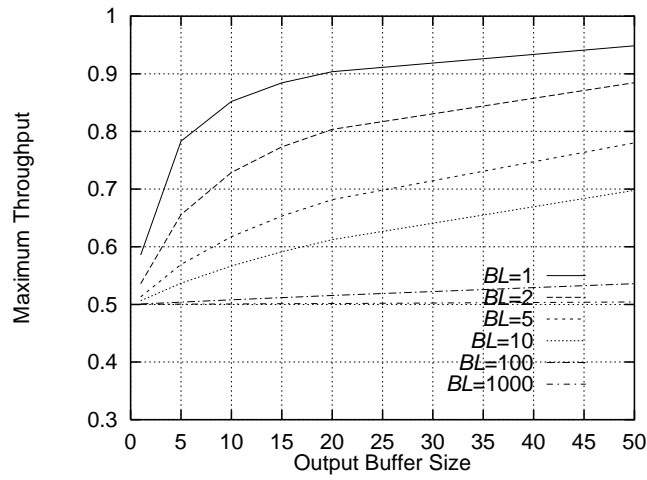


Figure 7: Maximum throughput vs. the output buffer size.

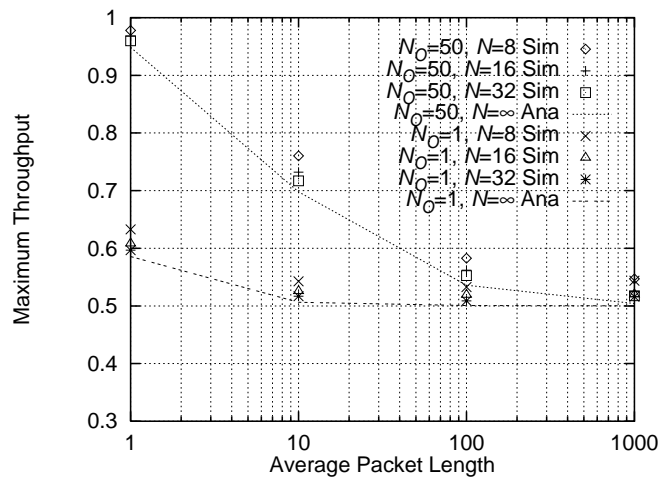


Figure 8: Comparison with simulation results.

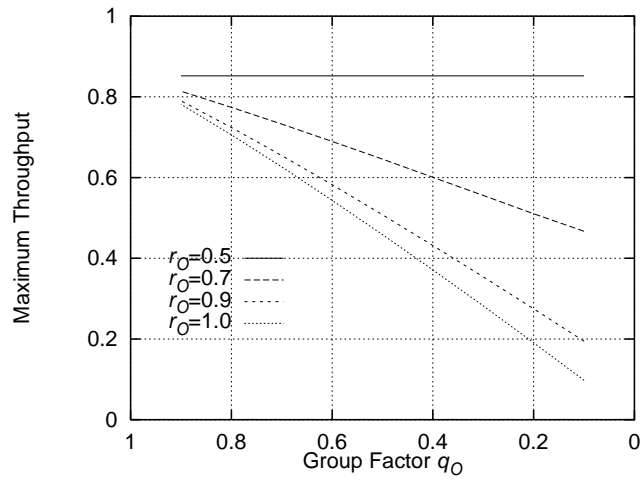


Figure 9: Unbalanced traffic at output ports ($N_O = 10, \overline{BL} = 1$).

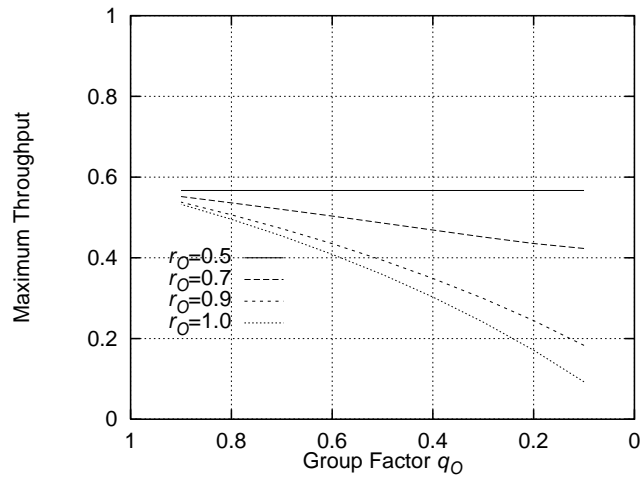


Figure 10: Unbalanced traffic at output ports ($N_O = 10, \overline{BL} = 10$).

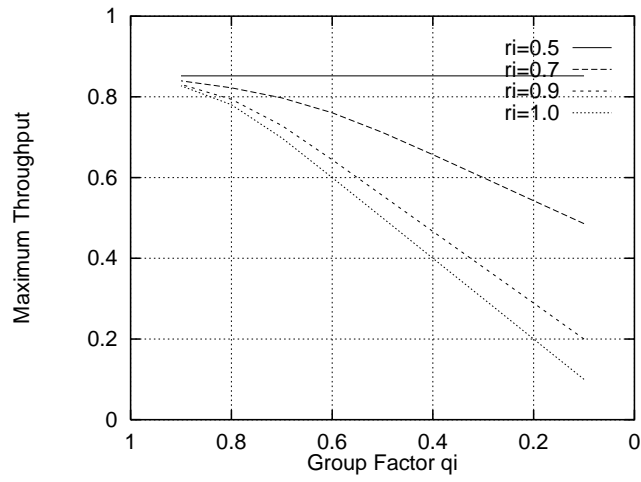


Figure 11: Unbalanced traffic at input ports ($N_O = 10, \overline{BL} = 1$).

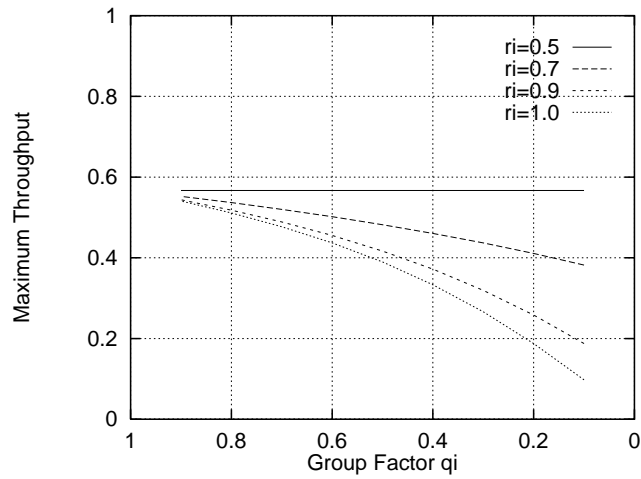


Figure 12: Unbalanced traffic at input ports ($N_O = 10, \overline{BL} = 10$).

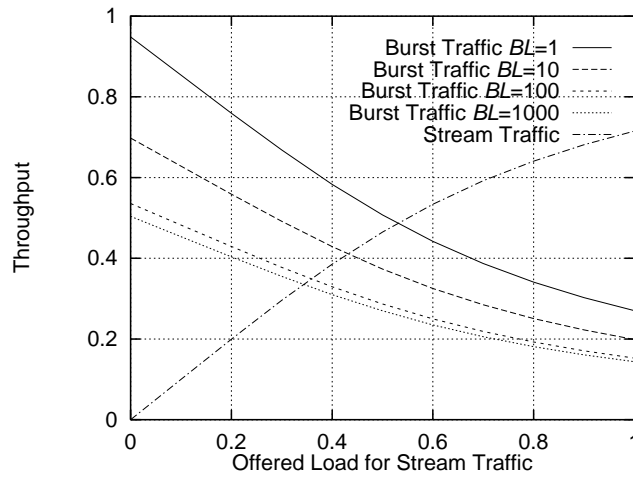


Figure 13: Throughput vs. the offered load of stream traffic.

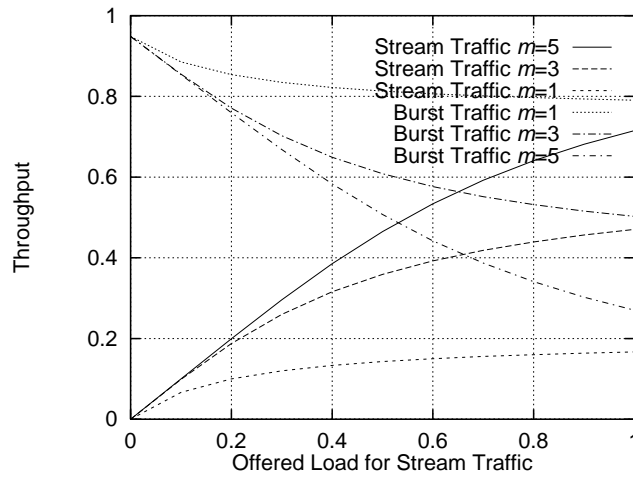


Figure 14: Effect of an available link capacity limitation on stream traffic.

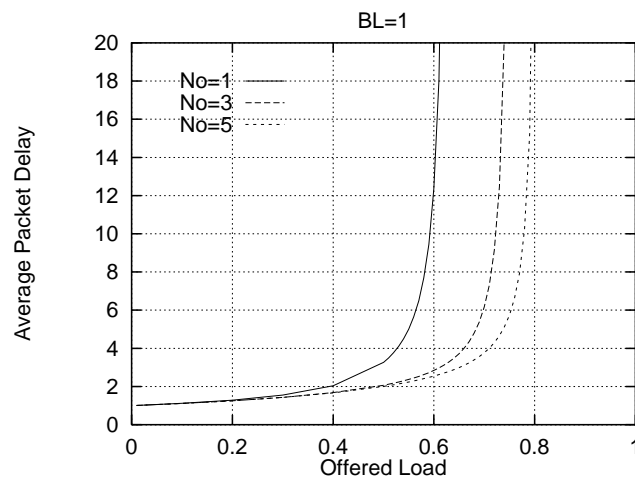


Figure 15: The average packet delay vs. the offered load for $\overline{BL} = 1$.

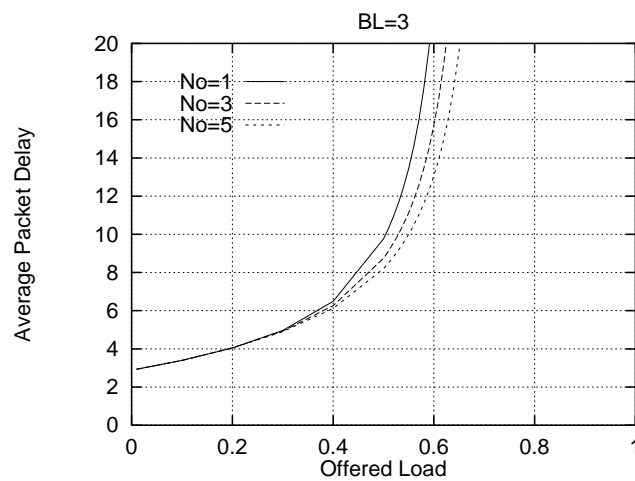


Figure 16: The average packet delay vs. the offered load for $\overline{BL} = 3$.

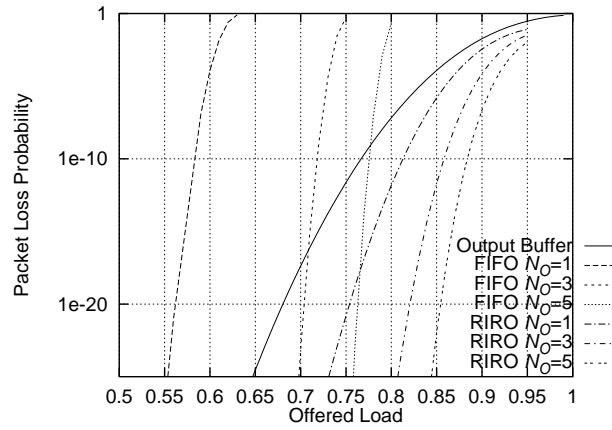


Figure 17: The packet loss probability vs. the offered load for $\overline{BL} = 1$.

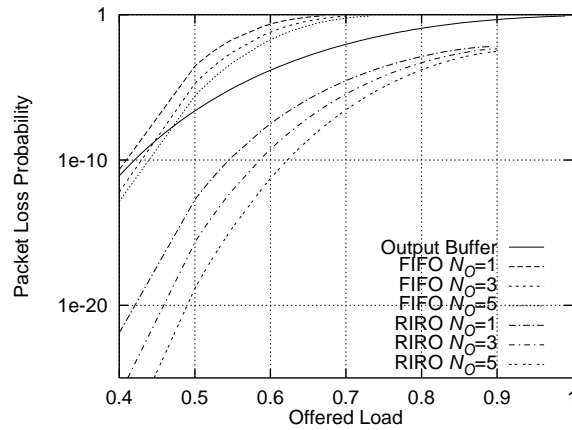


Figure 18: The packet loss probability vs. the offered load for $\overline{BL} = 3$.